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衛星通信における同期技術
－通信システムの安定動作のために－

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あらまし
通信網において最も広く用いられている同期技術は位相同期ループ(Phase-Lock-Loop, PLL)である。PLL は一旦同期を確立すると優れた追尾特性を有するが、その難点は引き込み動作、非同期状態に始まり同期状態に到る初期接続過程にある。即ち初期周波数誤差が大きいと同期過程に長大な時間がかかり、場合によっては同期に至らない事も起こる。この問題は低 C/N 条件ではより甚だしくなる。PLL の引き込み問題の原因は位相比較器の出力が位相誤差 θe に比例するものではなく sin(θe)に比例するものである事による。非同期時には位相比較器は周波数誤差 ωe に対して sin(ωe.t) (t は時間)なるビート波形を生じ、PLL は AFC 動作を行い、周波数誤差を縮小する。周波数誤差が同期範囲に入ると位相制御状態に移行し、同期が確立する。ここで問題は PLL の AFC 動作が不十分なところにある。本稿においては PLL の引き込み動作を解析し、その限界を明らかにする。次にその限界を打破する為に従来用いられてきた技術を紹介し、更に今後有望な技術を提案する。

キーワード　位相同期、PLL, 引き込み過程、引き込み時間、引き込み周波数範囲、AFC, APC, 複素信号, DSP

Synchronization Methods for Satellite Communications
(for stability of the systems)

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Abstract

The most widely used method for synchronization in communication systems is Phase-Locked-Loop (PLL). The PLL shows excellent tracking performances once the synchronization state is achieved. However, the problems of the PLL exist in its Pull-In process; it can take a long time or fail in achieving the synchronization state if the initial frequency difference is too large. The problem is enhanced in poor C/N conditions. The initial acquisition problem of the PLL comes from the fact that the phase detector gives a signal proportional to sin(θe) instead of θe which is the phase error. In the asynchronous state the phase detector gives a sine wave signal which frequency modulates the voltage controlled oscillator (VCO). In the asynchronous state the PLL functions as an automatic frequency control (AFC) device which achieves reduction of the frequency error to the range of Lock-In frequency where the PLL can achieve automatic phase control (APC) to establish the synchronization state. The problem comes from the poor AFC performance of the PLL. In this paper the pull-in process is analyzed to clarify the problem. Then some methods to improve the pull-in processes are described including some new methods. .

Keyword
Synchronization, Phase-Locked-Loop, PLL, Pull-in process, Lock-in range, AFC, APC, Complex signals, DSP

1. PLL in Satellite Communications

Phase-Lock-Loop (PLL) is a universal technology for synchronization used in vast areas in communications and controls systems. For communication satellites the PLL works in the critical components as frequency converters, timing generators and MODEMs. The onboard systems are required to be extremely reliable as repair of the components on the satellites is impossible once they are launched on the orbits. One such critical failure is a loss of synchronization by failure of a PLL subsystem. The PLL is a reliable component in steady state operations. It can fail in the pull-in process when the initial frequency difference is large especially in poor C/N conditions.

2. Pull-In Process of PLL

2.1 Structure of PLL

The structure of PLL is given in Fig 2-1.

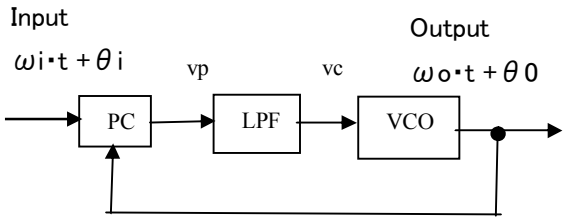

Fig 2-1 Structure of Phase-Lock Loop (PLL)

The PLL is composed of PC; phase comparator, LPF; loop filter and VCO; voltage controlled oscillator. The input signal is

$si(t) = \sin(\omega i \cdot t + \theta i)$

and the output signal so(t) is

$so(t) = \cos(\omega o \cdot t + \theta o)$

where ω, θ stand for the frequency and phase of the input and output signals.

The PC gives the output

$vp = Kp \cdot \sin(\omega e \cdot t + \theta e)$

where $\omega e = \omega i - \omega o$, and $\theta e = \theta i - \theta o$.

Kp is the phase detection sensitivity (V/rad).

The phase detector output is smoothed by the LPF to give the control voltage vc to control the VCO. The VCO is an FM oscillator whose output frequency changes proportionally to the control voltage vc.

$\omega o = \omega f + kv \cdot vc$

where ωf is free run frequency and Kv (rad/sec/V) is the FM sensitivity of the VCO.

2.2 Function of PLL

The function of PLL is analyzed by the following figure.

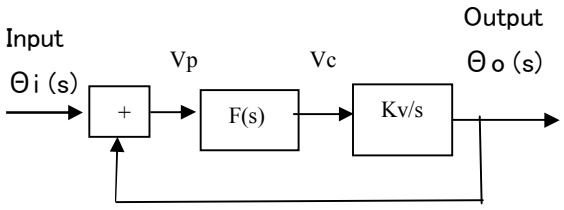

Figure 2-2. Functional Block Diagram of PLL

Where Θi(s), Θo(s) are the Laplace transforms of the phases of the input and output signals. Note the VCO functions as an integrator; the impulse response of which is;

$[0, \infty] \int e^{-(s \cdot t)} dt = 1/s$

A typical loop filter is

$F(s) = \alpha + 1 / (s \cdot \tau)$

2.2.1 PLL functions in synchronization state

In synchronization (steady) state the PLL functions in linear modes; the phase comparator gives approximately $Kp \cdot \Theta e$ ($\Theta e = \theta e = \theta i - \theta o$, $\omega e = 0$). Then the open loop transfer function of PLL is

$$\Theta o(s) = K0 \cdot (\alpha + 1 / (s \cdot \tau) / s \cdot \Theta e$$
$$= Go(s) \cdot (\Theta i - \Theta o).$$

Where $Ko = Kp \cdot Kv$ (1/sec) is the loop gain of the PLL. Go(s) is the Open-Loop transfer function.

The closed loop transfer function of the PLL is

$$H(s) = \Theta o / \Theta i = Go(s) / (1 + Go(s))$$
$$= (2\zeta \cdot \omega n \cdot s + \omega n^2) / (s^2 + 2\zeta \cdot \omega n \cdot s + \omega n^2)$$

Where $\omega n = \sqrt{(Ko / \tau)}$; natural angular frequency

$\zeta = 1/2 \cdot \alpha \cdot \sqrt{(Ko \cdot \tau)}$; damping factor.

Thus the function of the PLL in steady state is an LPF.

Width the bandwidth; $BL = \omega n/2 \cdot (\zeta + 1/(4\zeta))$

2.2.2 Pull-In Process of PLL

When the synchronization is not achieved yet, the phase comparator gives a beat signal;

$$vp = Kp \cdot \sin(\omega e \cdot t + \theta e)$$

The loop filter output is;

$$vc = \alpha \cdot vp + Vint$$

where Vint is the voltage integrated by the loop filter.

The control voltage vc controls the frequency of the VCO with the free run frequency ; ωf.

$$\omega o = \omega f + Kv \cdot Vc$$

$$= \omega f + \alpha \cdot Ko \cdot \sin(\omega e \cdot t + \theta e) + Kv \cdot Vint$$

$$= \omega F + \alpha \cdot Ko \cdot \sin(\omega e \cdot t + \theta e)$$

Where

$$\omega F = \omega f + Kv \cdot Vint$$

is the average frequency of the VCO output.

The frequency error is;

$$\omega e = \omega i - \omega o$$

$$= \Delta\omega - \alpha \cdot Ko \cdot \sin(\omega e \cdot t + \theta e)$$

$$= \Delta\omega - \omega L \cdot \sin(\Theta e)$$

Where

$\omega L = \alpha \cdot Ko$; Lock -in frequency

$\Delta\omega = \omega i - \omega F$; Average frequency error

$\Theta e = \omega e \cdot t + \theta e$

As

$$d\Theta e / dt = \omega e$$

The above relationship is rewritten;

$$d\Theta e / dt = \Delta\omega - \omega L \cdot \sin(\Theta e)$$

Apparently a steady state; $d\Theta e / dt = 0$, can be achieved

if $|\Delta\omega| < \omega L$

and the residual phase error Θes;

$$\Theta es = \arcsin(\Delta\omega / \omega L)$$

hence ωL is called Lock-In frequency.

2.2.3 AFC function of PLL

When $|\Delta\omega| > \omega L$, there is no steady state and the phase comparator gives a sinusoidal wave. The one cycle period Te of the beat signal is obtained as follows;

$$dt = 1 / \{\Delta\omega - \omega L \cdot \sin(\Theta e)\} d\Theta e$$

$$Te = [0, 2\pi] \int 1 / \{\Delta\omega - \omega L \cdot \sin(\Theta e)\} d\Theta e$$

$$= 2\pi / \Delta\omega \ / \sqrt{(1 - (\omega L / \Delta\omega)^2)}$$

The sinusoidal component contains a DC component Vfd which gives frequency discrimination voltage.

$$Vfd = 1/Te \cdot \int \alpha \cdot Kp \cdot \sin(\Theta e)\, dt$$

$$= 1/Te \cdot [0, 2\pi] \int \alpha \cdot Kp \cdot \sin(\Theta e) / \{\Delta\omega - \omega L \cdot \sin(\Theta e)\}\, d\Theta e$$

$$= \alpha \cdot Kp \cdot \Delta\omega / \omega L \cdot (1 - \sqrt{(1 - (\omega L / \Delta\omega)^2)})$$

This voltage is applied to the VCO to reduce the frequency error by the amount of ωfc.

$$\omega fc = \Delta\omega \cdot (1 - \sqrt{(1 - (\omega L / \Delta\omega)^2)})$$

which is depicted in the following figure.

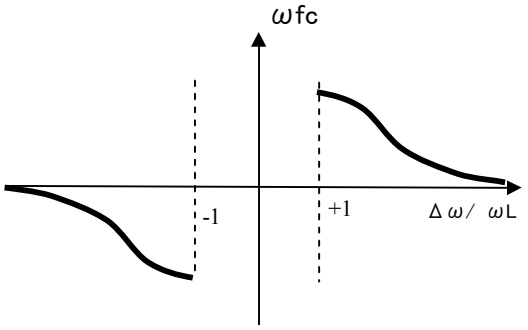

Fig.2-3 Frequency Discrimination Characteristics

AFC Loop

The above correction frequency ωfc is integrated by the loop filter and controls the VCO in the AFC Loop as depicted in the following figure.

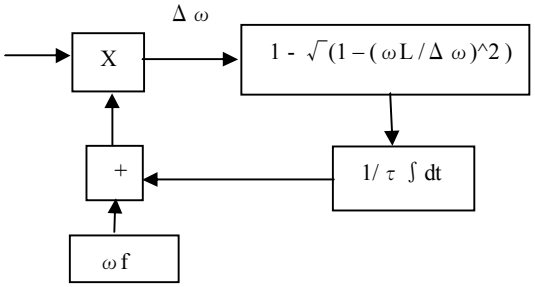

Fig.2-4 AFC Loop of PLL in Pull-in Process

The AFC loop of the PLL in the Pull-in process is ruled by the differential equation;

$$d\Delta\omega / dt = -1/\tau \cdot \Delta\omega \cdot (1 - \sqrt{(1 - (\omega L / \Delta\omega)^2)})$$

The pull-in time Tp is given by;

$Tp / \tau = [\omega L, \ \Delta \omega o] \int d(\Delta\omega) /(\Delta\omega \cdot (1 - \sqrt{(1 - (\omega L /\Delta\omega)^2))}$

$=[1, \ \Delta \omega o / \omega L] \int (x + \sqrt{(x^2 - 1)}) dx$

$> 1/2. ((\Delta \omega o / \omega L)^2 - 1)$

$< (\Delta \omega o / \omega L)^2 - 1$

Therefore the pull in time in the case the initial frequency error $\Delta\omega o$ is much greater than the Lock-in frequency ωL is given by ;

$Tp (=) \ \tau \cdot (\Delta \omega o / \omega L)^2$

Similar results are given by Viterbi [Ref. 1].

3. PLL with Enhanced AFC

The weakness of the PLL in the pull-in process had been studied and various methods have been used. One group of methods enhance the AFC functions of the PLL.

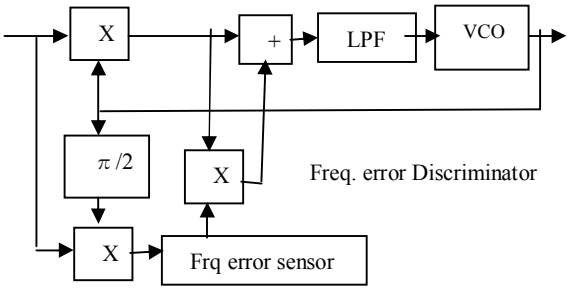

Fig. 3-1 PLL with enhanced AFC

Lindsay describes the method which uses a differentiator for the frequency error sensing device [Ref.2]. The author developed methods that use Low Path Filters for the frequency error sensors [Ref.3, 4]. Those methods proposed by the author have shown excellent performances in low C/N conditions.

The frequency error is detected as follows.

The first phase comparator gives the output;

$vp = A \cdot \sin (\omega e \cdot t + \theta e)$

The output of the second phase comparator is;

$vq = A \cdot \cos (\omega e \cdot t + \theta e)$

For the frequency error sensor, we use a simple low pass filter with the time constant Td and the transfer function; $1 / (1+ s \cdot Td)$.

Then the output of the frequency error sensor is;

$vq' = A/\sqrt{(1+(\omega e.Td)^2)}. \cos (\omega e.t + \theta e - \arctan (\omega e.Td))$

Then the frequency discriminator gives

$Vfd = vp \cdot vq'$

$= A \cdot \sin (\omega e.t + \theta e)$

$\cdot A/\sqrt{(1+(\omega e.Td)^2)}. \cos (\omega e.t + \theta e - \arctan (\omega e.Td))$

$= A^2 / \sqrt{(1+(\omega e.Td)^2)} \cdot \sin(\arctan (\omega e.Td))$

$= A^2 \cdot \omega e.Td \ / \ (1+(\omega e.Td)^2)$

which gives a good frequency discrimination performance.

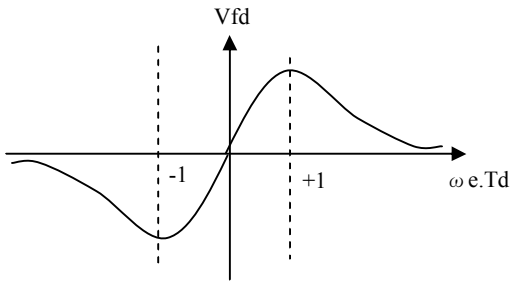

Fig.3-2 Frequency Discrimination Characteristics of the LPF Baseband Frequency Discriminator

As the frequency sensing device is a low pass filter, it is robust against thermal noise.

4. Complex PLL

The essence of the above enhanced AFC technology is the use of the complex signals.

$e^{(j\Theta)} = \cos(\Theta) + j.\sin(\Theta) \qquad (j^2 = -1)$

The idea can be further extended to realize a fully complex PLL as described in the following.

4.1 Transient response of an LPF

Let be a pair of Low-pass filters with identical transfer functions;

$Lc(s) = 1 / (1+ s.Tc)$

Apply a complex signal wi(t) to the filter with the initial wi(0) = 0. .

$wi(t) = \ e^{ (j(\omega e.t + \theta e))}$

Then the output response is

$wo(t) = e^{j(\theta e - \arctan(\omega e.Tc)) / \sqrt{(1+(\omega e.Tc)^2)}}$

$\cdot (e^{(j \omega e.t)} - e^{(-t / Tc)})$

The response signal is in different time scale is

$wo(t) = \ 0 \qquad (t=0)$

$= \ t / Tc \cdot e^{(j(\omega e.t+ \theta e))} \qquad (t << Tc)$

$= \ e^{j(\ \omega e.t + \theta e - \arctan(\omega e.Tc))}$

$/ \sqrt{(1+(\omega e.Tc)^2)} \qquad (t>>Tc)$

Note that the output response in short time after the input of the signal is

$$wo(t) = t / Tc \cdot wi(t)$$

That is the output signal phase is exactly that of the input signal.

4.2 Complex PLL ; Basic Structure

The above fact suggests that a complex PLL with fast processing time can be realized with a perfect phase error detection capability. Furthermore, the circuit can be implemented in a perfect digital signal processing (DSP) circuitry. A bock diagram is shown in Fig.4-1. In the figure all elements function in complex manners.

Suppose we have two complex variables ; $w = x + jy$, $c = a + jb$.

Then the signal processing are made as follows;

Addition ; $w + c = (x + a) + j(y + b)$

Multiplication $w \cdot c = (a.x - b.y) + j(a.y + b.x)$

Note a complex multiplication requires four real multiplications.

Another basic element in the complex PLL is the integrator.

Let the input be ; $vi(n) = e^{(j \theta i(n))}$ (n-th sample)

And the output ; $vo(n) = e^{(j \theta o(n))}$

Conduct the following complex multiplication;

$$vo(n) = vi(n) \cdot vo(n-1)$$

In terms of the phase, it is the addition as follows;

$$\theta o(n) = \theta i(n) + \theta o(n-1)$$

In Z-transform

$$\Theta(z) = [n= 0, \infty] \Sigma \theta(n) \cdot z^{(-n)}$$

($z = e^{(s.Ts)}$; Ts is the time period of the DSP processing)

$$\Theta o(z) = \Theta i(z) + z^{(-1)} \cdot \Theta o(z)$$

Or

$$\Theta o(z) / \Theta i(z) = 1/ (1 - z^{(-1)})$$

For $t << Ts$, this is nearly equal (denoted by (=))

$$\Theta o(z) / \Theta i(z) = 1/ (1 - e^{(-s.Ts)})$$

$$(=) (1/Ts) / s$$

namely an integrator with gain 1/Ts.

The complex PLL depicted in Fig.4-1 is composed of the complex processing devices; adders and multiplies as above described..

4.3 Functions of Complex PLL

In terms of the phases of the signals, the multiplication of the complex signals is equivalent to addition of the phase. The equivalent functional block diagram in terms of the signals phases is given by Fig. 4-2.

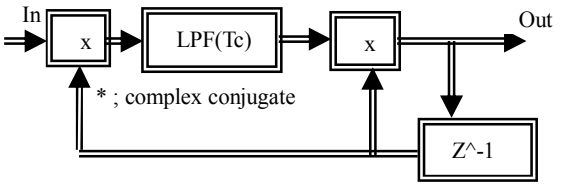

Fig. 4-1 Structure of Complex PLL

Note the LPF(Tc) is transparent in terms of the phase.

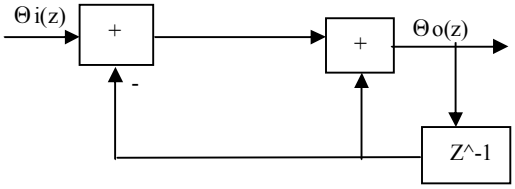

Fig 4-2 Functional Block Diagram of Complex PLL

(First order type)

The transfer function of of the complex PLL is achieved as follows.

$$\Theta o(z) = \Theta e(z). z^{-1}/ (1- z^{-1})$$

$$\Theta e(z) = \Theta i(z) - \Theta o(z)$$

The transfer function is simply

$$\Theta o(z) / \Theta i(z) = z^{-1}$$

Namely the output signal phase is simply that of the input signal delayed only by one sample.

One slight problem is the steady state error.

For the frequency error ωe;

$$\theta i(n) = \omega i. Ts.n + \theta e$$

$$\theta o(n) = \theta i(n-1)$$

$$= \omega i. Ts.(n-1) + \theta e$$

The steady state phase error is

$$\theta es(n) = \theta i(n) - \theta o(n)$$

$$= \omega i. Ts$$

The steady state phase error can cause problems in some applications that require very small phase errors, e.x. MODEMs.

The above phase error remains because the complex PLL is the first

order type PLL. As well known the steady state phase error of the PLL can be removed by a secondary order PLL with a perfect integrator. The functional block diagram of the second order complex PLL is given in the figure.

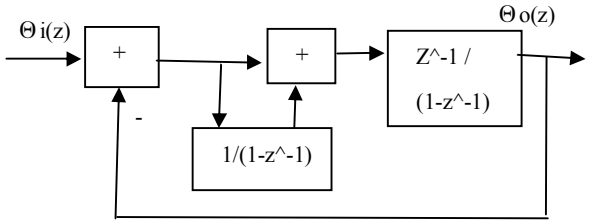

Fig.4-3 Second Order Complex PLL

The transfer function of the second order complex PLL is now obtained.

$$\Theta o(z) = \Theta e(z).\{1 + 1/(1-z^{-1})\}.\ z^{-1}/(1- z^{-1})$$

$$\Theta e(z) = \Theta i(z) - \Theta o(z)$$

The transfer function is

$$\Theta o(z) / \Theta i(z) = z^{-1} \cdot (2 - z^{-1})$$

In the time domain

$$\theta i(n) = \omega i.\ Ts.n + \theta e$$

$$\theta o(n) = 2\theta i(n-1) - \theta i(n-2)$$

$$= \omega i.\ Ts.n + \theta e$$

$$= \theta i(n)$$

Hence the phase error is

$$\theta e(n) = \theta i(n) - \theta o(n)$$

$$= 0$$

4.4 Fully digital implementation of the complex PLL

The proposed complex PLL can be fully digitally implemented.

In addition to the complex adders and multipliers, the LPF(Tc) can be also implemented by DSP devices as follows.

The transfer function of the LPF

$$L(z) = 1 / (1 - \alpha \cdot z^{-1}) \qquad (0 < \alpha < 1)$$

$$= 1 / (1 - \alpha \cdot e^{(-s.Ts)})$$

$$(=) 1 / (1 - \alpha) / \{1 + \alpha.Ts / (1 - \alpha) \cdot s\}$$

Which is equivalent to LPF(Tc) with the time constant Tc;

$$Tc = \alpha.Ts / (1 - \alpha)$$

4.5 Noise performances

The input signal has additive thermal noise which is Additive, White and Gaussian Noise (AWGN) with broad bandwidth Bi.

The input signal is a sum f the signal and AWGN ni(t).

$$wi(t) = A \cdot \sin(\omega i \cdot t + \theta i) + ni(t)$$

The input C/N is

$$[C/N]i = (A^2 / 2) / (No.Bi)$$

where No is the noise power density (W/Hz) and Bi the noise bandwidth (Hz).

The C/N is maintained in the complex multiplier that functions as phase comparator. The C/N is then improved by the low path filter $Lc(s) = 1 / (1 + s.Tc)$. The bandwidth of the LPF is;

$$Bc = 1/ (2\pi.Tc) \qquad (Hz)$$

Thus the C/N at the output of LPF(Tc) is

$$[C/N]c = [C/N]i\ .\ Bi / Bc$$

It is expected that this gives the C/N of the output signal of the proposed complex PLL.

Conclusions

The problems of PLL in the pull-in processes were reviewed. The pull-in process mechanism was analyzed by a simple model. Some field-proven methods to enhance the AFC functions of the PLL in the initial acquisition are described. The essence of those technologies is processing of complex signals. A new type of PLL totally of complex signal processing is proposed. The complex PLL can be implemented in perfect DSP circuitry. The proposed complex PLL is not field-proven yet. The author expects the new generations of engineers will improve the technology to realize PLL with perfect pull-in capability.

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